CONCURRENT PROCESSOR ARRAY FOR HIGH SPEED ROUTE PLANNING

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Abstract

A VLSI parallel processor array for high speed optimal route planning is reported. Based on programmed terrain costs (traversal time), the IC determines the fastest routes from a selected starting point(s) to all other points on a given terrain. Based on the successful demonstration of a prototype 24 x 25 VLSI processor chip (1), a cascadable 64x 64 processor array is currently under development and will be presented in this paper.

Introduction

The problem of determining the fastest route between two points for a given terrain is computationally intensive. For many applications, such as defense or civilian emergency dispatching, computation time is critical. This paper reports the integration of a random access array of digital processors which arc programmed to model a given terrain and determine the fastest (lowest cost) path between any points on the terrain at very high speed (tens of microseconds for arrays up to 1024 x 1024). The primary purpose of this chip is to provide high speed path planning capability for tactical mobility analysis in battlefield scenarios. However such high speed automated path planning will find utility in a variety of settings such as autonomous vehicle navigation, intelligent vehicle highway systems, evacuation and rescue planning, and police and transportation dispatching.

Currently, the only tools available to assist in path planning arc implemented in software. These approaches can be slow, with best path determination typically requiring seconds to minutes for terrain size.s varying from 64 x 64 to 1024 x 1024 pixels (2). Through the VLSI implementation of a fine grain parallel architecture, in which every terrain pixel is represented by a corresponding processor, the inherent parallelism of the problem can be exploited and extremely fast path determination can be realized.

This paper describes the development of a 64 x 64 cascadable parallel processor IC for route planning over complex terrain. Based on the successful demonstration of a 24 x 25 research chip, the 64 x 64 IC greatly surpasses the prototype chip in both array size and capability, enabling the fabrication of a 1024 x 1024 route planning coprocessor (accelerator) board for incorporation into an existing tactical mobility system.

Array Architecture and Operation

The path planner architecture, shown schematically in Fig. 1, consists of a 64 x 64 array of unit cell processors which communicate with their nearest neighbors and are random] y accessed by 6-bit row and column decoders located adjacent to the array. The digital IC implemented in a single-poly, double-metal, 0.8 pm, CMOS, n-well process utilizes custom design and layout to minimize processor size.

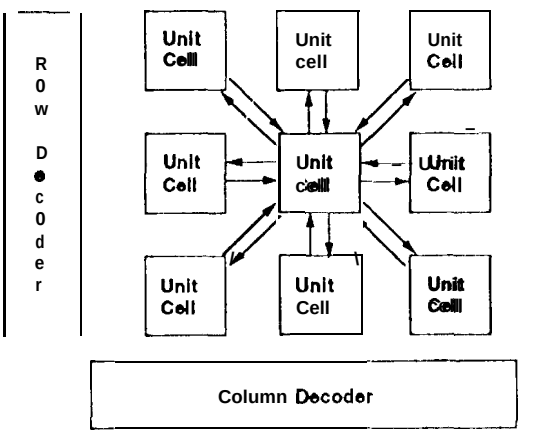

Fig. 1 Block diagram of IC architecture.

In order to determine the fastest routes from a selected start ing point(s) to all other points on a given terrain, each unit cell processor corresponds to a terrain grid pixel which has been preprogrammed with the costs (i.e. delays) of traveling to each of its eight neighboring pixels. The unit Cell, shown schematically in Fig. 2 occupies 249 µm x 264.5 pm. Operation begins with the selection of a path origination pixel(s) which sends out a signal to its eight neighbors. After a signal is received, the incoming signal direction is stored, further inputs to the cell arc disabled, and the signal is broadcast to each of its neighbors after a preset delay (unique delay for each direction).

Signal propagation through the array, controlled by the variable cell to cell delays, are implemented with eight counters per unit cell - one for each outgoing direction. Each of the eight 5-bit ripple down counters are preset to